WHAT IS CLAIMED IS:

1. A data storage device comprising:

a first memory cell string that includes at least a first memory cell coupled to a second memory cell; and

a circuit coupled to a node between the first memory cell and a second memory cell, the circuit configured to detect a voltage change at the node in response to a voltage being provided to the memory cell string and the first memory cell being written to a first state.

2. The data storage device of claim 1 wherein the circuit is configured to detect that the first memory cell was in a second state prior to being written to the first state in response to detecting the voltage change.

3. The data storage device of claim 2 wherein the circuit is configured to cause the first memory cell to be written to the second state subsequent to detecting the voltage change.

4. The data storage device of claim 2 wherein the circuit is configured to cause a logic level associated with the second state to be read out.

5. The data storage device of claim 1 wherein the circuit is configured to detect that the first memory cell was in the first state prior to being written to the first state in response to not detecting the voltage change.

6. The data storage device of claim 5 wherein the circuit is configured to cause a logic level associated with the first state to be read out.

7. The data storage device of claim 1 wherein the first memory cell string has a first end and a second end, wherein the voltage is provided to the first end, and wherein the second end is coupled to a ground source.

8. The data storage device of claim 7 further comprising:

a second memory cell string that includes a third memory cell coupled to a fourth memory cell; and

wherein the second memory cell string has a third end and a fourth end, and wherein the third end and the fourth end are coupled to the ground source in response to the first memory cell being written to the first state.

9. The data storage device of claim 7 wherein the first memory cell is coupled to the first end, and wherein the second memory cell is coupled to the second end.

10. The data storage device of claim 7 wherein the first memory cell is coupled to the second end, and wherein the second memory cell is coupled to the first end.

11. The data storage device of claim 7 wherein the memory cell string includes a third memory cell and a fourth memory cell, and wherein the first, the second, the third, and the fourth memory cells are coupled in series.

12. A method of performing a read operation from a first memory cell in a memory cell string that includes the first memory cell and a second memory cell comprising:

providing a voltage to the memory cell string;

measuring a first voltage at a node between the first and second memory cells;

writing the first memory cell to a first state;

measuring a second voltage at the node; and

determining whether the first voltage differs from the second voltage.

13. The method of claim 12 further comprising:

determining that the first memory cell was in a second state prior to being written to the first state in response to the first voltage differing from the second voltage.

14. The method of claim 13 further comprising:

reading out a logic level associated with the second state in response to the first voltage differing from the second voltage.

15. The method of claim 13 further comprising:

writing the first memory cell to the second state in response to the first voltage differing from the second voltage.

16. The method of claim 12 further comprising:

determining that the first memory cell was in the first state prior to being written to the first state in response to the first voltage not differing from the second voltage.

17. The method of claim 16 further comprising:

reading out a logic level associated with the first state in response to the first voltage not differing from the second voltage.

18. A system comprising:

a first memory cell;

a second memory cell coupled to the first memory cell;

a transistor coupled to a node between the first and second memory cells and coupled to a bit line associated with the first memory cell;

a means coupled to the bit line for detecting a voltage change at the node in response to:

a first voltage being provided to the first and second memory cells;

the first memory cell being written to a first state; and

a second voltage being provided to the transistor.

19. The system of claim 18 wherein the transistor comprises a voltage follower transistor.

20. The system of claim 18 wherein the transistor includes a gate connection, a source connection, and a drain connection, wherein the gate connection is coupled to the node, and wherein the source connection is coupled to the bit line.

21. The system of claim 18 wherein the transistor includes a gate connection, a source connection, and a drain connection, wherein the source connection is coupled to the node, and wherein the drain connection is coupled to the bit line.

22. The system of claim 18 wherein the transistor includes a gate connection, a source connection, and a drain connection, wherein the drain connection is coupled to the node, and wherein the source connection is coupled to the bit line.

23. The system of claim 18 wherein means is for detecting that the first memory cell was in a second state prior to being written to the first state in response to detecting the voltage change, and wherein the means is for causing a logic level associated with the second state to be read out.

24. The system of claim 18 wherein the means is for detecting that the first memory cell was in the first state prior to being written to the first state in response to not detecting the voltage change, and wherein the means is for causing a logic level associated with the first state to be read out.

25. The system of claim 18 a voltage source configured to provide the first voltage and the second voltage.